PCB Project: Measuring Package Bond-Out Inductance via Ground Bounce

Kylan Roberson
EE173

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Abstract

In this experiment I looked into a way of measuring the ground bounce generated by capacitively loading 5 outputs of a Texas Instrument small outline package Hex-Flip Flop chip and discharging them all simultaneously. Using these measurements I determined a package wirebond inductance using two methods, one provided by Graham & Johnson and one developed in this paper. The Graham & Johnson method determined a package inductance of 0.52 nH while the method described in this paper determined an inductance of 0.495 nH. These values deviated by 15% and 10% respectively from what was reported in the TI package performance app-note [3], and therefore for the purposes of this experiment it was determined that the method explained in this paper is more appropriate for determining ground bounce.

1 Introduction

Ground bounce occurs as the result of package wirebond having a non-zero inductance. This means there is a non-zero inductance between physical ground and the ground reference on a chip. Note that inductors act as high impedances to quickly changing currents given by the inductive relationship:

$$V = L\frac{dI}{dt}$$

For a large current time derivative the inductance kicks up a large voltage. Observe also that the current generated by a discharging capacitance is expressed according to the relationship:

$$I = C\frac{dV}{dt}$$

Charging a capacitive load on the outputs of a package, and then simultaneously disgchargin all of them through the package will induce a time varying current equal to the capacitively scaled time derivative of the voltage discharge.

Notice that the voltage across the bond-out inductance to ground alters the internal ground reference of the package. It is clear to see that changing the ground reference changes the voltage of an output tied to the internal ground of the package with respect to the ground plane. We would like to measure and consider the maximum or peak value of this changing ground reference which is determined like so:

$$V_{gnd\,\max} = L\frac{dI_{\max}}{dt}$$

The source of high speed current switching, as we explained previously, is the capacitive discharge current. We can replace the current in the differential with the capacitive differential voltage used to describe discharge current:

$$V_{gnd\,\max} = LC\left(\frac{d^2V}{dt^2}\right)_{\max}$$

Finally we must make an assumption about the time domain geometry of the voltage V. As we have discussed in class, high speed digital signals are typically gaussian. If we treat the digital output of our logic family as gaussian pulses and find where the second derivative of the gaussian pulse is maximum, then we can determine what this maximum should be. Graham and Johnson give us an empirical equation for determining the maximum of this second derivative, parameterized in terms of peak voltage and 10%-90% rise time:

$$\left(\frac{d^2V}{dt^2}\right)_{\max} = 1.52\left(\frac{V_p}{T_{10-90}^2}\right)$$

We can substitute this into our ground bounce equation for a final computable result:

$$V_{gnd\,\max} = 1.52 \cdot LC \cdot \left(\frac{V_p}{T_{10-90}^2}\right)$$

We would like to determine the package inductance by measuring the ground bounce for a variety of capacitive loads. Since the ground bounce is linearly dependent on the capacitance, what we can do is take a linear fit of the capacitance vs. ground bounce magnitude and solve for the slope. The inductance can then be easily solved as:

$$L = \frac{T_{10-90}^2}{1.52 \cdot V_p} \cdot \text{slope}$$

Before proceeding we would like to verify the emperical equation theoretically. Note that the gaussian pulse has a sigmoid geometry determined by the erf() function. If we take a unit amplitude erf() centered at $1/2$ so that the signal asymptotically approaches 0 on the left and 1 on the right like so:

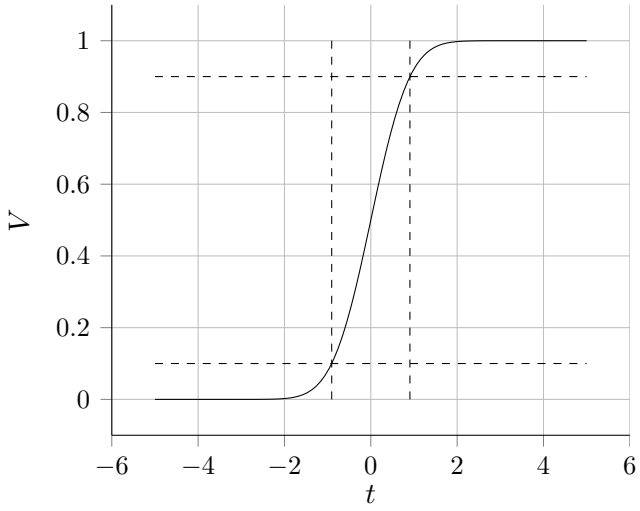

Figure 1: Gaussian edge with a 10-90 rise marked

Setting these conditions allows us to more simply solve for the 10-90 rise time T_{10-90} by setting our erf() equation equal to 0.1 and 0.9 in `Mathematica`'s equation solver. There is not a closed form solution to this problem, and using computer aided approximation is the simplest way to get around this. `Mathematica` gives us solutions of $t = \pm\ 0.906$, in other words a T_{10-90} of 1.812.

We then take the second derivative of the erf() function and use `Mathematica` to solve for the maximum explicitly (this is the point where concavity maximizes). The antisymmetric behavior plotted below is precisely the behavior we expect to see as ground bounce:

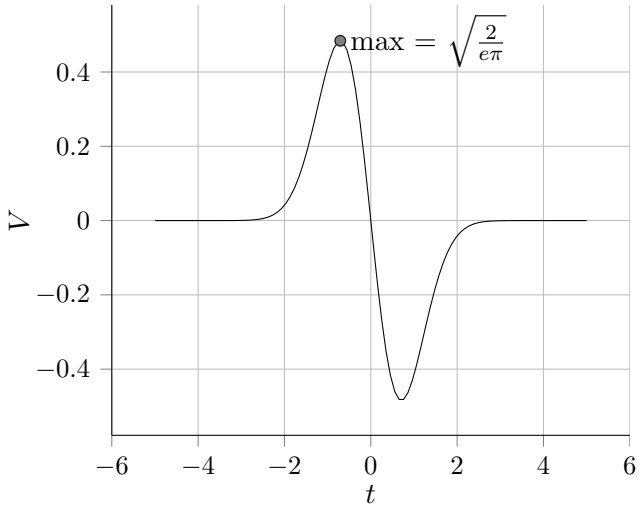

Figure 2: second derivative of the gaussian pulse with maximum identified by `Mathematica`.

The maximum of the second derivative of our gaussian signal was determined to be $\sqrt{\frac{2}{e\pi}} \approx 0.484$. With our computed values, we want to determine a coefficient β such that:

$$\left(\frac{d^2V}{dt^2}\right)_{\max} = \beta\left(\frac{V_p}{T_{10-90}^2}\right)$$

Here V_p is unity, therefore β is simply:

$$\beta = T_{10-90}^2 \cdot \left(\frac{d^2V}{dt^2}\right) = (1.812)^2 \cdot \sqrt{\frac{2}{e\pi}} \approx 1.59$$

Since diffirentiation is linear, any rise time or voltage amplutide scaling factor should not alter this relative coefficient.

We can see that this is in slight disagreement with the 1.52 that Graham and Johnson reported. In fact, it is 4.4% different. The purpose of my experiment is to see which version of the equation gives a more appropriate determination of package inductance and attempt to verify the empirical validity of Graham and Johnson's equation. The 4.4% is very small and I suspect that it may be too small to resolve which equation is more adequate,

but the original motivation I had for my experiment was to understand why Graham & Johnson picked 1.52 and whether their reasoning could be reproduced.

If our experiment does not demonstrate the validity of either of these equations, it could mean one of two things: either there were unaccounted for factors in our experiment that prevented us from resolving ground bounce properly *or* the high speed capacitive discharge is *not* gaussian shaped.

2 Materials & Methods

The following is a schematic of my design:

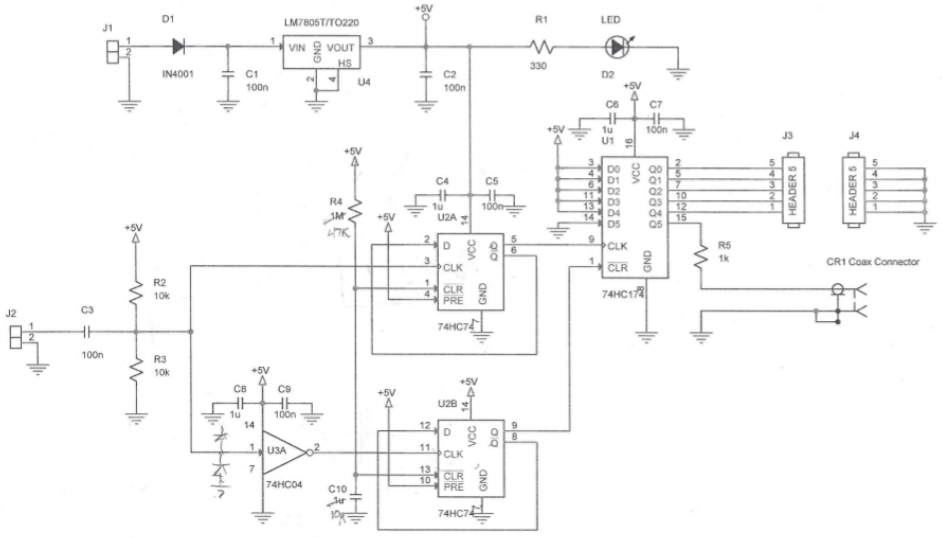

Figure 3: Ground bounce circuit schematic.

I used the HC logic family with a 5V regulator, since the max rated supply voltage to the HC device was 6V and the available 6V regularor had error margins that exceeded this. Each HC chip was bypassed with a 1 μF and 100 nF parallel capacitance. These were chosen to handle lower and higher frequency noise on the power rail, where a single capacitance would only bypass one of these noise ranges.

The sig gen was set to a 1V, 15 kHz square wave and applied to a trace biased to $^1/_2\, V_{cc}$ which is used to clock a state machine (the source swing can be kept low because of the biasing). The state machine generates a 90° offset clock and clear signal which is sent to a Hex Flip flop package with 5 inputs tied high and 1 tied low. Ideally, we want the data to be clocked in, then at a quarter of the clock period, an active low clear signal is asserted and the high outputs, which are capacitively loaded, discharge through the package and a ground bounce can be observed on the always low output.

There is a slight error in the logic design of this control system. The clear signal is asynchronous. At power initialization, an RC delay is used to pull the active low clear signals of the flip flops from ground to V_{cc}. The preset signal is pulled high and therefore both flip flops start in the state Q = 0. An inverter on the clock input of one of the flops is used to generate the 90 degree shift. However, when the reset signal goes high relative to the clock level is non-deterministic. Therefore the phase shift can be 90 degrees in either direction (i.e. the active low clear to the hex flip flops can lead the clock signal by a quarter period, or follow. Proper operation only occurs where the posedge of the reset leads the posedge of the clock). When the clear signal is pulled high while the clock is low, the generated clock will incorrectly lead the generated clear. As a result of the asynchronous design and non-deterministic nature of when the clear signal goes high relative to the clock, the state machine is non-deterministic and 50% of the time it will produce incorrectly timed outputs. To get around this, we briefly shorted the RC delay line enough times until the correct bahavior was produced. A proper design solution to this problem will be discussed later.

Finally, we generated different capacitive loads by hooking the hex flip flop outputs to 5 sets of sockets that we were able to plug axially leaded

capacitors into. We chose to look at how loading the output between 10 pF and 75 pF would affect the ground bounce magnitude. To measure this, I probed the reset signal and triggered the scope on the negative edge since it is active low. The oscillation seen here corresponded to when the capacitively loaded outputs were reset and discharged through the chip.

3 Results & Analysis

When I hooked the board up with no capacitive load and triggered off the reset I saw the following behavior:

Figure 4: Ground bounce plotted under the reset signal displayed at a resolution of 5 V per tick. The time was 10 ns per tick and the voltage for the ground bounce was 5 mV per tick

As can be seen, there is ringing which I measured to oscillate at 167 MHz. When a capacitive load was placed on the design, I observed that the first peak of this ringing was increased while the rest of the ringing was attenuated. I assumed that this first peak which was 13.2 mV above the ground plane corresponded to the ground bounce and measured the difference in gain between when the chip was capacitively loaded and unloaded

C (pF)	$V_{gnd\ \max}$ (mV)
5	2.2
10	3.0
15	3.8
25	3.6
30	5.1
40	5.9
45	8.1
55	8.2
60	8.9
75	9.1

to determine $V_{gnd\ \max}$.

The following table contains the measured ground bounce amplitude changes and the respective capacitive load:

We generated a linear fit of this data in `gnuplot` and determined a slope of 0.1095 $^{\text{mV}}/_{\mu\text{F}}$ with a coefficient of determination of 0.93, giving a 7% uncertainty in the linear relationship of our data.

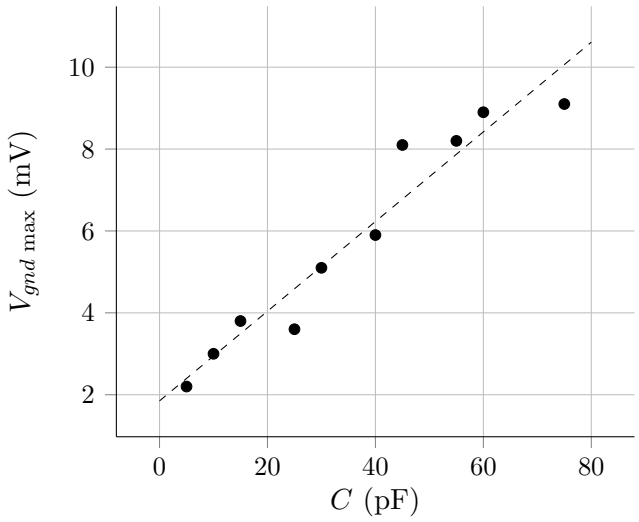

Figure 5: linear fit of measurements with slope of 0.1095

The logic was driven at 5 V meaning the switching voltage V_p was 5 V. I also determined the 10-90 fall time was about 6 ns which matched the information on the datasheet. Using the computed slope I calculated an inductance according to the equation provided by Graham and Johnson:

$$L = \frac{T_{10-90}^2}{1.52 \cdot V_p} \cdot \text{slope} = \frac{(6\text{ ns})^2}{1.52 \cdot 5\text{ V}} \cdot 0.1095\ {}^{\text{mV}}/_{\mu\text{F}} \approx 0.52\text{ nH}$$

I then calculated an inductance according to the theoretically determined method equal to 0.496 nH and compared both calculations against a wirebond inductance reported by Texas Instruments [3, p. 7] of 0.45 nH.

We can see that the Graham & Johnson method results in a value that is 15.3% different from the reported inductance while the theoretical method developed in this paper is only 10.2% different. Therefore, at least for the purposes of this experiment, the theoretical method generates a more appropriate result in better agreement with the manufacturer's notes.

4 Conclusion & Future Improvements

I was able to generate somewhat conclusive results with my board as noted by the relative percent deviation between the two methods of calculating wirebond inductance compared with the values reported in the TI app-note. My experiment demonstrated that the theoretical considerations made in determining wirebond inductance more closely modeled expected behavior than the empirical equation provided by the authors of our text. This indicates that the discharge geometry is likely gaussian shaped. The 10% deviation is still a somewhat large deviation, however I believe the primary source for this was a result of capacitor lead inductance. The reason I think this to be the case was because when I loaded the output with skinnier leaded capacitors of higher nominal capacitance (i.e. 25 pF vs 15 pF) it did not increase the ground bounce behavior like I predicted. The sockets also may have introduced obsticles and unaccounted for effects. When the outputs were not driving capacitive loads, the oscillation I observed was relatively high, when it should not have been. I think they may have introduced some

lumped ringing behavior that made it harder to resolve what was ground bounce and what wasn't.

Ultimately, however, I wish I had had the foresight to use onboard capacitive banks. I noticed other people get much better and more conclusive results with less ringing by hooking up switches to banks of surface mount capacitors (which have significantly lower lead inductance compared to axially leaded capacitors). While it would not offer the same dynamic range of output loading that using sockets did, I think the parasitic effects of my experiment overshadowed some of the behavior I was aiming to see and in the end being able to swap around capaitive loads ended up not being as beneficial as I imagined.

It is interesting that I was able to get somewhat conclusive results. I was eager to try and verify the emperical nature of the equation provided by Graham and Johnson. But as it turned out, I instead concluded that their equation was not better than the theoretically computed one.

Finally, as noted earlier, the control logic of my design needs to be redesigned in order to properly deterministically generate the correct signal timing. To do this, I must simply drive the reset signal into a flop with input pulled high which is clocked at the same rate as the two flops of the state machine and drive the output of the reset flop to the reset of those same two flops as dipicted:

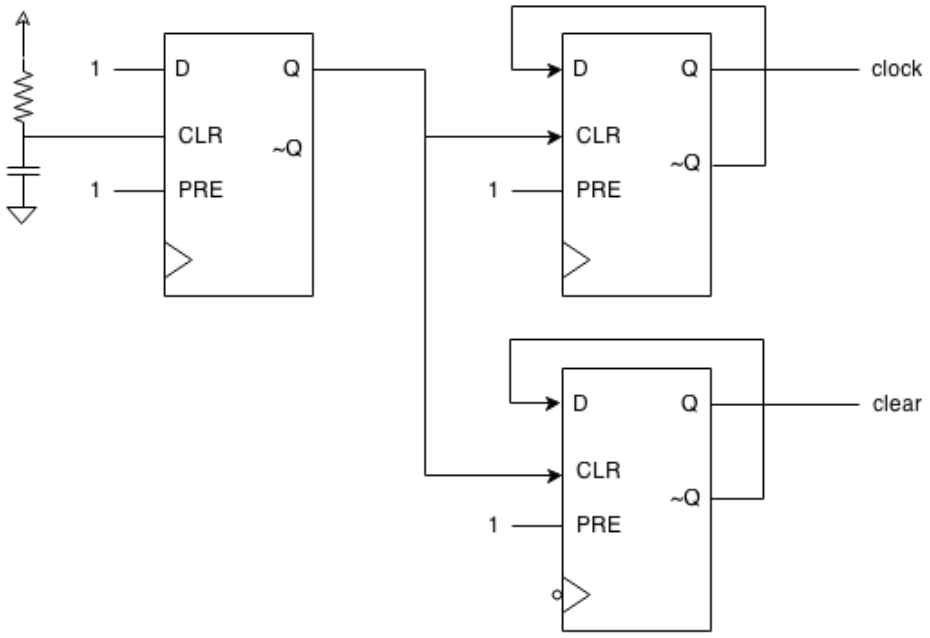

Figure 6: state machine with synchronous reset hardware diagram. The clock network is not shown for simplicity.

In other words, the RC reset is driven into a flop which will only update on the positive clock edge. Therefore we deterministically esure that a transition from active reset to reset high happens only when the clock is high.

There may be design considerations that I have not fully accounted for, however. For instance clock skew may cause behavioral problems where the reset signal clocks high before the clock has reached the state machine flops, which would imply a reset transition occuring when the clock is still low in the state machine and would lead to the incorrectly timed behavior. However, if the flops are kept in close proximity with one another, the clock skew should not be a serious issue. Something else to note is that this design improvement introduces extra complexity, since a separate dual flip flop package would need to be added to the board. However, this is a perfectly acceptable cost to always ensure proper design execution and not

risk destroying components by shorting power and ground to fiddle out the correct signalling.

References

[1] S.C. Petersen, *Experiment 4: PCB Project*, Santa Cruz, California: Jack Baskin School of Engineering, 2014.

[2] M. Graham, H. Johnson, *High-Speed Digital Design: A Handbook of Black Magic*, Upper Saddle River, New Jersey: Prentice Hall PTR, 1993.

[3] Texas Instruments Inc., *AN-1205 Electrical Performance of Packages*, May, 2004.